## **IN THE CLAIMS**

## Please amend claim 1 as follows:

1. (Three Times Amended) A method of forming a CMOS sidewall spacer, comprising the steps of:

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forming a PMOS transistor gate structure on a n-type region of a semiconductor substrate;

forming a NMOS transistor gate structure on a p-type region of said semiconductor substrate;

forming initial single layer sidewall structures of similar widths adjacent to said NMOS transistor gate structure and said PMOS transistor gate structure; and

etching said initial single layer sidewall structure adjacent to said NMOS transistor gate structure such that the width of the single layer sidewall structure adjacent to said NMOS transistor gate structure is less than the width of the single layer sidewall structure adjacent to said PMOS transistor gate structure.